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Signed this 19th day of January, 2005

CHAE, JUNGSOOK

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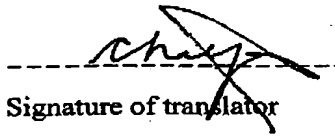

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【Abstract】

The present invention relates to a method for fabricating a semiconductor device capable of forming fine patterns through the application of a photoresist trimming technique and improving a gap-fill property during deposition of a bit line insulation layer through decreasing line widths of line patterns such as bit lines by employing an ArF photolithography process. To achieve these effects, the method includes the steps of: forming a hard mask insulation layer on an etch target layer; forming a hard mask sacrificial layer on the hard mask insulation layer; coating a photoresist on the hard mask insulation layer; selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern; selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width; removing the photoresist pattern; etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width; and etching the etch target layer by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width, wherein the first width is wider than the fourth width by at least about 20 nm.

【Selected Drawing】

Fig. 2d

【Index words】

Argon fluoride (ArF), bit line, photoresist pattern trimming, tungsten, sacrificial hard mask, line pattern

【Specification】

【Title of the Invention】

METHOD FOR FABRICATION OF SEMICONDUCTOR DEVICE CAPABLE OF FORMING FINE PATTERN

【Brief Description of the Drawings】

Figs. 1a to 1f are perspective views illustrating serial processes for forming line type storage nodes.

Figs. 2a to 2d are cross-sectional views illustrating serial processes for forming line patterns of a semiconductor device by using a light source of F_2 or ArF in accordance with a preferred embodiment of the present invention.

Figs. 3a to 3d are micrographs of scanning electron microscopy (SEM) showing cross-sectional views and top views of semiconductor structures each obtained through the corresponding individual processes depicted in Figs. 2a to 2d.

Fig. 4 is a graph showing changes in a critical dimension (CD) in each etching step illustrated in Figs. 2a to 2d.

Fig. 5 is a micrograph of SEM showing a cross-sectional view of bit lines each with a line width of approximately 70 nm.

Fig. 6 is a graph showing a decremental change in a CD i.e., a third line width (W3) according to etching time when a hard mask is formed as shown in Fig. 2c.

*Description of the Principal Reference Numerals

20: substrate 21b: conductive pattern

22c: hard mask W1: DICD

W4: FICD

【Detailed Description of the Invention】

【Object of the Invention】

【Field of the Invention and the Related Prior Art】

The present invention relates to a method for fabricating a semiconductor device; and more particularly, to a method for forming a fine pattern, especially, a bit line, capable of decreasing a critical dimension (CD).

Generally, a semiconductor device includes various internal unit devices. Large scale of integration has led these unit devices, e.g., a transistor and a capacitor, to be formed densely within a predetermined cell area. Thus, the size of the unit devices has been gradually decreased as well. Particularly, in a semiconductor device like a dynamic random access memory (DRAM) device, the design rule has been also shifted toward a trend of minimization, further resulting in a decrease in the size of semiconductor devices. For instance, a currently fabricated semiconductor DRAM device has a minimum line width below about 0.1 μm, and thus, there arise many difficulties in forming semiconductor unit devices corresponding to this technical advance.

Hereinafter, a method for forming line type storage nodes

disclosed in Korean Laid-Open No. 2000-0045869 by S. C. Park, P. G. Kong and K. H. Yoon, entitled "Method for Fabricating Contact Hole and Spacer of Semiconductor Device" will be described in detail. Figs. 1a to 1f are perspective views illustrating a method for forming the line type storage nodes.

Referring to Fig. 1a, a conductive layer 11 for forming a bit line (hereinafter referred to as the bit line conductive layer) is formed on a substrate 10 providing various unit devices such as transistors and word lines. An insulation layer 12 for a hard mask (hereinafter referred to as the hard mask insulation layer) is deposited on the bit line conductive layer 11. Then, a plurality of first photoresist patterns 13 for defining the width of the bit line is formed on the hard mask insulation layer 12.

Herein, the bit line conductive layer 11 is typically formed by using one of tungsten (W), tungsten silicide (WSi_x), titanium silicide ($TiSi_x$), cobalt silicide ($CoSi_x$), aluminum (Al) and copper (Cu). The hard mask insulation layer 12 serves to protect bit line patterns or gate electrode patterns in the course of forming contact holes by etching a typical inter-layer insulation layer. Thus, the hard mask insulation layer 12 is made of a material having a significantly different etching rate from that of the inter-layer insulation layer. For instance, if the inter-layer insulation layer is made of an oxide-based material, silicon nitride or silicon oxynitride is used for the hard mask insulation layer 12. If the inter-layer insulation layer is

made of a polymer-based low dielectric material, an oxide-based material is used for the hard mask insulation layer 12.

A photoresist pattern 13 for specifying a width of a bit line is formed on the hard mask insulation layer 12.

Referring to Fig. 1b, the hard mask insulation layer 12 is etched by using the first photoresist pattern 13 as an etch mask to form a plurality of hard masks 12a. Thereafter, the first photoresist pattern 13 is removed by a photoresist stripping process.

Next, the bit line conductive layer 11 is then etched by using the hard masks 12a as an etch mask so to form bit lines each having a stack structure of the hard mask 12a and the conductive pattern 11a.

Meanwhile, the aforementioned photoresist stripping process can be performed after the bit line conductive layer 11 is etched.

Referring to Fig. 1c, an inter-layer insulation layer 14 made of an oxide-based material is formed on an entire surface of the resulting substrate structure including the bit lines.

Next, as shown in Fig. 1d, a second photoresist pattern 15 for defining contact hole regions is formed on the inter-layer insulation layer 14. At this time, the second photoresist pattern 15 is formed by using a line type mask pattern.

Referring to Fig. 1e, the inter-layer insulation layer 14 is etched by using the photoresist pattern 15 as an etch mask

to form contact holes 16 each exposing a predetermined portion of the substrate 10 allocated between the conductive patterns 11A, i.e., the bit lines. Herein, the contact hole 16 is for a storage node contact.

Also, since the conductive patterns 11a are bit lines, said each exposed portion of the substrate 10 during the formation of the contact holes 16 corresponds to a plug conductive layer contacted to a source/drain junction region of the substrate 10. However, this plug conductive layer is not shown for the sake of simplified explanation.

Referring to Fig. 1f, an etch stop layer 17 is formed in the form of spacers on sidewalls of each bit line.

The etch stop layer 17 is made of a typical nitride-based material since the etch stop layer 17 is for preventing losses of the hard masks 12a and the conductive patterns 11a during a subsequent etching process as like the function of the hard masks 12a.

For the process for forming line type contact holes as described above, the width W of the bit line and the thickness D of the hard mask 12a serve important functions.

For instance, if the width W of the bit line is large, a gap-fill property may be degraded when the inter-layer insulation layer 14 is deposited, and an aspect ratio may increase.

To solve the problems of the increase in the aspect ratio and the degradation of the gap-fill property, there is suggested a method for decreasing the width W of the bit line

to improve the aspect ratio.

However, when a line type mask pattern, e.g., a self-aligned contact (SAC) mask pattern, is applied based on sub-0.1 μm integration technology, it is difficult to gap-fill the inter-layer insulation layer 14, i.e., the bit line insulation layer, between the bit lines without generating voids. Thus, it is required to reduce a critical dimension (CD) of the bit line to secure gap-fill margins by improving the aspect ratio.

Recently, this approach of decreasing the CD of the bit line has been focused greatly since the decreased CD of the bit line makes it possible to provide a solution to the gap-fill property degradation, increase an area of the bottom plug and form the etch stop layer for use in the spacer with a sufficient thickness.

However, it is compulsory to develop appropriate photolithography for decreasing the CD of the bit line, and a photo-exposure process is one important process for achieving such effects.

Hence, such a laser as ArF having a wavelength of about 193 nm is used as a light source for a photolithography process to attain the above described effects. However, it is not easy to secure the CD of about 0.1 μm in consideration of the fact that the minimum realizable width is about 0.08 μm even with use of the ArF. Also, the required width of the bit line is about 0.055 μm in order not to bring out the above mentioned problems, and thus, the current advance in

the development of the photolithography is not enough to achieve intended outcomes.

For this reason, there is currently suggested a photoresist trimming technique for reducing the CD by inducing losses of the photoresist pattern with appropriate use of an etch gas after the formation of the photoresist pattern.

In other words, the photoresist trimming technique is an etching technique for obtaining a final inspection critical dimension (FICD) of the photoresist pattern narrower than a develop inspection critical dimension (DICD) of the initially formed photoresist pattern.

At this time, the photoresist trimming technique adopts the fact that the width of the photoresist pattern is decreased by performing a plasma etching process due to characteristics of the material used for forming the photoresist. Typically, a plasma containing chlorine (Cl_2), hydrogen bromide (HBr) and oxygen (O_2) gas is used. More specifically, a predetermined portion of the photoresist pattern is etched by using a gas of Cl_2/O_2 or HBr/O_2, and then, a hard mask beneath the photoresist pattern is etched by using the etched photoresist pattern as an etch mask.

However, in case of employing an ArF photolithography technique applicable to sub-0.1 μm technology, an ArF photoresist is severely deformed when the ArF photoresist is etched by using the aforementioned $Cl_2/HBr/O_2$ plasma. Also, the photoresist trimming technique employing such ArF

photolithography technique has several limitations in fabricating highly integrated semiconductor memory devices like DRAMs.

【Objects of the Invention】

It is, therefore, an object of the present invention to provide a method for fabricating a semiconductor device capable of forming fine patterns by applying a photoresist trimming technique.

It is another object of the present invention to provide a method for fabricating a semiconductor device capable of improving a gap-fill property during deposition of an insulation layer by narrowing a line width of a line pattern such as a bit line.

It is further another object of the present invention to provide a method for fabricating a semiconductor device through the use of an ArF photolithography technique capable of minimizing a line width of a line pattern.

【Configuration of the Invention】

In accordance with one aspect of the present invention, there is provided a method for fabricating a semiconductor device, including the steps of: forming a hard mask insulation layer on an etch target layer; forming a hard mask sacrificial layer on the hard mask insulation layer; coating a photoresist on the hard mask insulation layer; selectively performing a photo-exposure process and a developing process

to form a photoresist pattern having a first width for forming a line pattern; selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width; removing the photoresist pattern; etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width; and etching the etch target layer by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width, wherein the first width is wider than the fourth width by at least about 20 nm.

In accordance with another aspect of the present invention, there is provided a method for fabricating a semiconductor device, including the steps of: forming a hard mask insulation layer on an etch target layer; forming a hard mask sacrificial layer on the hard mask insulation layer; forming an anti-reflective coating layer on the hard mask sacrificial layer; coating a photoresist on the anti-reflective coating layer; selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern; etching the anti-reflective coating layer by using the photoresist pattern as an etch mask; selectively etching the hard mask sacrificial layer with use of the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width; removing the photoresist pattern and

the anti-reflective coating layer; etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width; and etching the etch target layer by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width, wherein the first width is wider than the fourth width by at least about 20 nm.

In accordance with further aspect of the present invention, there is provided a method for fabricating a semiconductor device, including the steps of: forming a conductive layer containing tungsten on a substrate; forming a hard mask insulation layer on the conductive layer; forming a hard mask sacrificial layer containing tungsten on the hard mask insulation layer; forming a photoresist pattern having a first width on the hard mask sacrificial layer to form a line pattern; selectively etching the hard mask sacrificial layer with use of the photoresist pattern as an etch mask to form a sacrificial hard mask having a second with; removing the photoresist pattern; etching the hard mask insulation layer with use of the sacrificial hard mask as an etch mask by controlling excessive etching conditions to thereby form a hard mask having a third width; and etching the conductive layer by using the sacrificial hard mask and the hard mask as an etch mask to form a line type conductive pattern having a fourth width, wherein the first width is wider than the fourth width by at least about 20 nm.

In order to minimize a line width of a line type conductive pattern, e.g., a bit line, etch gases and other process conditions are controlled in the course of etching an upper sacrificial hard mask containing tungsten and a nitride-based bottom hard mask. Therefore, it is possible to form fine patterns without being impacted by F_2 or ArF photolithography causing severe pattern deformation.

【Description of the Invention】

Hereinafter, with reference to the drawings, a preferred embodiment of the present invention will be explained in detail.

Figs. 2a to 2d are cross-sectional views illustrating serial processes for forming line type patterns of a semiconductor device by using a light source of F_2 or ArF in accordance with a preferred embodiment of the present invention.

Also, Figs. 3a to 3d are micrographs of scanning electron microscopy (SEM) showing cross-sectional and top views of substrate structures each obtained through the corresponding individual processes depicted in Figs. 2a to 2d.

Although the preferred embodiment of the present invention exemplifies a process for forming conductive line patterns, particularly, bit lines, it is still possible to apply the present invention to formation of other conductive patterns such as gate electrode patterns, storage node contacts and metal lines.

Referring to Fig. 2a, a conductive layer 21a, which is an etch target layer, is formed on a substrate 20 providing unit devices such as transistors and word lines. Then, an insulation layer 22a for use in a hard mask (hereinafter referred to as the hard mask insulation layer) is deposited on the conductive layer 21a. Herein, the hard mask insulation layer 22a is made of a nitride-based material such as SiON or Si_3N_4 having an insulating characteristic and a specific selectivity value with respect to the etch target layer, i.e., the conductive layer 21a or of a thin layer obtained by using an oxide-based material such as silicon oxide (SiO_2). Subsequent to the deposition of the hard mask insulation layer 22a, a sacrificial layer 23a for use in a hard mask (hereinafter referred to as the hard mask sacrificial layer) is formed on the hard mask insulation layer 22a in order to prevent pattern deformation caused by losses of the hard mask insulation layer 22a.

Herein, the hard mask sacrificial layer 23a is made of a material selected from a group consisting of polysilicon, Al, W, WSi_x, WN, Ti, TiN, $TiSi_x$, TiAlN, TiSiN, Pt, Ir, IrO_2, Ru, RuO_2, Ag, Au, Co, TaN, CrN, CoN, MoN, $Mosi_x$, Al_2O_3, AlN, $PtSi_x$ and $CrSi_x$. Also, all of the subscripts x representing a corresponding atomic ratio range from about 1 to about 2. Also, at this time, the hard mask sacrificial layer 23a is deposited to a thickness allowing an easy removal of the hard mask sacrificial layer 23a when the conductive layer 21a is etched. Preferably, the thickness of the hard mask

sacrificial layer 23a ranges from about 500 Å to about 3000 Å. The hard mask insulation layer 22a has a thickness preferably ranging from about 500 Å to about 5000 Å.

In addition, it is preferred that the conductive layer 21a is made of the same material used for forming the hard mask sacrificial layer 23a, i.e., the W contained material, in order not to perform an additional process for removing the hard mask sacrificial layer 23a. However, it is still possible to omit the process for removing the hard mask sacrificial layer 23a even without using the same material by controlling the thickness and etching conditions based on etch selectivity values of each employed material.

More specifically, the conductive layer 21a is made of a material selected from a group consisting of W, WSi_x, $TiSi_x$, $CoSi_x$, Al and Cu. The hard mask insulation layer 22a is for protecting bit line patterns or gate electrode patterns in the course of forming contact holes by etching a typical inter-layer insulation layer, and thus, the hard mask insulation layer 22a is made of a material having significantly different etching rate from the inter-layer insulation layer. For instance, if the inter-layer insulation layer is made of an oxide-based material, the hard mask insulation layer 22a is made of a nitride-based material such as Si_3N_4 or SiON. If a polymer-based low dielectric material is used for the inter-layer insulation layer, the hard mask insulation layer 22a is made of an oxide-based material.

Furthermore, the substrate 20 includes insulating structures and conductive structures. Particularly, if the conductive layer 21a is used for bit line patterns or metal lines as shown in the preferred embodiment of the present invention, there are formed plugs each comprising at least one of a diffusion barrier layer made of Ti and TiN, an impurity junction region such as a source/drain, an inter-layer insulation layer, a polysilicon layer and a W layer on an interface between the conductive layer 21a and the substrate 20. If the conductive layer 21a is for forming gate electrode patterns, a gate insulation layer (not shown) is formed on an interface between the conductive layer 21a and the substrate 20.

An anti-reflective coating (ARC) layer 24 is formed on the hard mask sacrificial layer 23a to prevent formation of undesired patterns caused by scattered reflection created by high reflectance of the hard mask sacrificial layer 23a during a photo-exposure process for forming patterns on the hard mask sacrificial layer 23 and to improve adhesion between the hard mask sacrificial layer 23a and a photoresist which will be subsequently coated.

Herein, the ARC layer 24 is formed with an organic material having similar etching characteristics with the photoresist. Thus, it is preferable to form the ARC layer 24 with a thickness ranging from about 100 Å to about 1000 Å.

After the deposition of the ARC layer 24, a photoresist made of cyclic olefin maleic anhydride (COMA) or acrylate is

coated on the ARC layer 24 by performing a spin coating technique. Herein, the photoresist is for use in F_2 or ArF photolithography. A predetermined portion of the photoresist is then selectively photo-exposed by using a light source of F_2 or ArF and a predetermined reticle (not shown) for defining the width of a bit line. Thereafter, a developing process makes photo-exposed portions or non-photo-exposed portions remain, and a cleaning process is performed to remove etch remnants, thereby forming a plurality of first photoresist pattern 25a.

The denotations W1 and d1 express the width of the first photoresist pattern 25a and a spacing distance between the first photoresist patterns 25a. Thus, as depicted in the sections (a) and (b) of Fig. 3a, the width W1 is a develop inspection critical dimension (DICD) of a bit line to be subsequently formed. Also, the W1 and the d1 are referred to as the first width and the first spacing distance hereinafter.

Referring to Fig. 2b, the ARC layer 24 is selectively etched by performing an etching process with use of the first photoresist patterns 25a as an etch mask. At this time, a chlorine-based plasma such as Cl_2, BCl_3, CCl_4 or HCl is used as an etch gas to attain a trimming effect with minimizing deformation of the first photoresist patterns 25a. It is also preferable to add O_2 gas to this etch gas.

In case of using a reactive ion etching (RIE) apparatus, top and bottom portions of a reaction chamber are supplied with different powers ranging from about 400 W to about 800 W

and from about 70 W to about 130 W, respectively, and a pressure within the reaction chamber is maintained in a range from about 6 mTorr to about 12 mTorr. Also, when a mixed gas of Cl_2 and Ar is used, it is preferable to use the Cl_2 and Ar each with a quantity ranging from about 35 sccm to about 65 sccm and from about 20 sccm to about 50 sccm, respectively.

Next, the hard mask sacrificial layer 23a is etched by using the first photoresist patterns 25a and the ARC layer 24 as an etch mask to form a plurality of sacrificial hard masks 23b.

If the hard mask sacrificial layer 23a is a tungsten (W) containing thin layer such like a tungsten (W) layer, a tungsten silicide (WSi_x) layer or a tungsten nitride (WN) layer, a plasma using a mixed gas of SF_6 and N_2 is used.

At this time, in case of using the RIE apparatus, top and bottom portions of the reaction chamber are supplied with different powers ranging from about 450 W and about 850 W and from about 30 W to about 60 W, respectively, and a pressure within the reaction chamber is maintained in a range from about 8 mTorr to about 16 mTorr. Also, it is preferable to use the SF_6 and N_2 each with a quantity ranging from about 7 sccm to about 13 sccm and from about 10 sccm to about 20 sccm, respectively.

Also, if the hard mask sacrificial layer 23a is a Ti containing thin layer such like a Ti layer, a TiN layer, a $TiSi_x$ layer, a TiAlN layer or a TiSiN layer, a chlorine-based gas, particularly Cl_2 gas, is used as a main etch gas. At

this time, O_2 or CF gas is added to the main etch gas to control an etch profile.

In case that the hard mask sacrificial layer 23a is a thin layer made of Pt, Ir, Ru or an oxide material of the above listed noble metals, a plasma containing chlorine-based gas or fluorine-based gas is used. At this time, it is necessary to use high ion energy to control the etch profile, and thus, a recipe of a low pressure and a high bias power is preferably maintained.

As shown in Fig. 2b, after the above etching process, each of the remaining photoresist patterns 25b has a second width W2 narrower than the first width W1 of the first photoresist pattern 25a due to the trimming effect. Hereinafter, the remaining photoresist pattern 25b is referred to as the second photoresist pattern. Conversely, a second spacing distance d2 between the second photoresist patterns 25b become wider than the first spacing distance d1 between the first photoresist patterns 25a Therefore, as shown in the sections (a) and (b) of Figs. 3b, the second width W2 decreases compared with the DICD of the bit line as shown in Fig. 3a.

Although a change in the width of each bit line in Fig. 2b is not in a great extent, it is possible to obtain a final inspection critical dimension (FICD) of the bit line decreased by about 20 nm with respect to the DICD.

Subsequently, a photoresist stripping process is performed to remove the second photoresist patterns 25b and

the ARC layer 24, and a cleaning process is then performed to remove etch remnants having polymer characteristics.

Referring to Fig. 2c, the hard mask insulation layer 22a is etched by using the sacrificial hard masks 23b as an etch mask so to form hard masks 22b.

Meanwhile, when a photolithography process using ArF or the like is applied, it is another target to prevent pattern deformation with use of the ArF photoresist. Thus, it is more effective to reduce the FICD in the course of forming the hard masks 22b than to perform the above process for forming the sacrificial hard masks 23b.

In case that the hard mask insulation layer 22a is a nitride-based layer, a plasma containing a mixed gas of tetrafluoride (CF_4), trifluoromethane (CHF_3), ethylene (C_2H_4), helium (He), argon (Ar) and oxygen (O_2) gas is used. At this time, if the RIE apparatus is used, a power in a range from about 400 W to about 800 W is supplied and a pressure within the reaction chamber is maintained in a range from about 35 mTorr to about 65 mTorr. Also, it is preferable to use the CF_4, CHF_3, Ar and O_2 gas each with a quantity ranging from about 25 ccm to about 65 sccm, from about 40 sccm to about 80 sccm, from about 50 sccm to about 100 sccm and from about 12 sccm to about 25 sccm, respectively.

As shown in Fig. 2c, the second width W2 of each sacrificial hard mask 23b is trimmed to a third width W3, which will be the width of each bit line region. Hereinafter, the remaining sacrificial hard mask having the third width W3

is denoted as 23c. In contrast to the narrowed width, a third spacing distance d3 between the remaining sacrificial hard masks 23c is wider than the second spacing distance d2 between the sacrificial hard masks 23b. Hence, as shown in the sections (a) and (b) of Fig. 3c, the third width W3 decreases in a great extent compared with the CD depicted in Fig. 3b.

Although a change in the width of the bit line is not pronounced in the process for forming the sacrificial hard masks 23b shown in Fig. 2b, a quantity of the O_2 gas used in etching the hard masks 22b and an over-etching time are controlled to control an extent of trimming each of the remaining sacrificial hard masks 23c shown in Fig. 2c, so that the final bit line have the FICD reduced by more than 20 nm from the DICD.

Furthermore, it is possible to prevent pattern deformation caused by an excessive etching of the first photoresist patterns 25b or the ARC layer 24 that is mandated to be used as an etch mask during the etching of the hard mask insulation layer 22a in case that the sacrificial hard masks 23b are not used as the etch mask.

Referring to Fig. 2d, the conductive layer 21a is selectively etched by using the remaining sacrificial hard masks 23c and the hard masks 22b as an etch mask to form a plurality of the bit lines each having a stack structure of the remaining hard mask 22c and the conductive pattern 21b.

At this time, the conductive layer 21a is made of the

same material to the hard mask sacrificial layer 23a in order to eliminate additional etching process for removing the remaining sacrificial hard masks 23c used as the etch mask. Even if the conductive layer 21a is made of a different material from the hard mask sacrificial layer 23a, it is still possible to omit the additional etching process for removing the remaining sacrificial hard masks 23c by controlling a thickness of the conductive layer 21a and the etching conditions, which cause the remaining sacrificial hard masks 23c to be removed during the etching of the conductive layer 21a. Also, it is possible to prevent losses of the hard masks 22b caused by the remaining sacrificial hard masks 23c, and thereby being able to prevent deformation of the conductive patterns 21b.

Herein, the etching conditions for the conductive layer 21a is same as those applied to the formation of the sacrificial hard masks 23b except for the quantity and etching time.

That is, in case of using the RIE apparatus, top and bottom portions of the reaction chamber are supplied with different powers ranging from about 450 W to about 850 W and from about 30 W to about 60 W, respectively. Also, a pressure within the reaction chamber is maintained in the same range of about 8 mTorr to about 16 mTorr. Additionally, it is preferable to use SF_6 and N_2 each with a quantity ranging from about 70 sccm to about 130 sccm and from about 14 sccm to about 22 sccm, respectively.

In Fig. 2d, the remaining hard mask 22c has a fourth width W4 trimmed from the third width W3 of the hard mask 22b. On the other hand, a fourth spacing distance d4 between the remaining hard masks 22c becomes wider than the third spacing distance d3 between the hard masks 22b. Herein, the decreased fourth width W4 is the FICD of the final bit line.

As described above, the diffusion barrier layer including the Ti layer and the TiN layer is formed on the interface between the conductive pattern 21b and the substrate 20. Thus, when the diffusion barrier layer is etched, a plasma containing a mixed gas of BCl_3 and Cl_2 is used.

At this time, in case of using the RIE apparatus, top and bottom portions of the reaction chamber are supplied with different powers ranging from about 400 W to about 550 W and from about 50 W to about 100 W, respectively, and a pressure within the reaction chamber is maintained in a range from about 7 mTorr to about 13 mTorr. Also, it is preferable to use the BCl_3 and Cl_2 each with a quantity ranging from about 7 sccm to about 13 sccm and from about 80 sccm to about 150 sccm, respectively.

Fig. 4 is a graph showing changes in a critical dimension for each step illustrated from Figs. 2a to 2d.

As shown, at the first step, the DICD, i.e., the first width W1, is about 95 nm, and this first width W1 changes to the second width W2 of about 92 nm after the sacrificial hard mask 23b formation. Thus, the trimming effect attained from the formation of the sacrificial hard mask 23b results in a

decrease of the CD by about 2 nm. Thereafter, the second width W2 of the sacrificial hard mask 23b changes to the third width W3 of about 77 nm. During the formation of the hard mask 22b formation, the trimming effect results in a decrease of the CD by about 15 nm.

Also, during the formation of the conductive pattern 21b, the fourth width W4 of the final bit line, i.e., the FICD, is about 72 nm obtained by the trimming effect. That is, the third width W3 decreases by about 5 nm.

In overall, since the DICD is about 95 nm and the FICD is about 72 nm, the DICD decreases by more than about 20 nm, thereby obtaining the reduced FICD of the final bit line.

Accordingly, in case of forming the bit lines through ArF lithography, it is possible to minimize the pattern deformation by using the sacrificial hard mask. Also, the final width, i.e., the FICD, of the bit line can be reduced by at least about 20 nm compared to the first width W1, i.e., the DICD of the bit line, by controlling use of the etch gas and targeted etch time.

Fig. 5 is a micrograph of SEM showing a cross-sectional view of bit lines with the line width of about 70 nm.

As shown, there are bit line patterns each including the hard mask 22c and the conductive pattern 21b. Even if the initial width of the bit line is about 95 nm by performing an ArF photolithography process, it is possible to decrease the final width of the bit line to about 70 nm or less than this value through a trimming technique.

Fig. 6 is a graph showing changes in a ratio of the excessively etched target with respect to the thickness of the hard mask during the formation of the hard mask shown in Fig. 2c.

As shown, the trimming is accelerated in proportion to the etching time. Each of marked points at about 40 %, about 60 % and about 100 % represents a period of performing additionally the excessive etching process around an end of point (EPO) for etching the hard mask insulation layer 22a.

Therefore, it is preferable to control the excessive etching time based on the thickness and material characteristics of the hard mask insulation layer 22a.

The line type conductive patterns fabricated according to the preferred embodiment of the present invention have the stack structure of the nitride-based hard mask and the sacrificial hard mask, which is the tungsten containing metal conductive layer. Compared with the initially applied photolithography process, appropriate control of the trimming achieved by correspondingly manipulating the etch gas and the excessive etching time provides advantages of preventing the pattern deformation and realizing the formation of more fine patterns. As a result of these advantages, it is further possible to achieve an increase in yield of semiconductor devices and cost-effective fabrication.

While the present invention has been shown and described with respect to the particular embodiments, it will be apparent to those skilled in the art that many changes and

modifications may be made without departing from the sprit and scope of the invention as defined in the appended claims.

【Effect of the Invention】

In accordance with the present invention, the disclosed method makes it possible to form very fine patterns that cannot be achieved by employing a conventional photolithography process. Also, there is additional effect in that pattern deformation is minimized through employing the photo-exposure technology with use of ArF or F_2.